AN ION-IMPLANTED 13 WATT C-BAND MMIC WITH 60% PEAK POWER ADDED EFFICIENCY

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Abstract- **A GaAs MMIC power amplifier that produces in excess of 13 watts of RF power at 60% peak power added efficiency operating in C-band has been developed. Output power over 12 watts at better than 52% PAE has been measured over a 23% fractional bandwidth. The nominal circuit has been designed using non-linear modeling techniques and optimized empirically through fabrication and analysis of an 18-element Taguchi orthogonal array of circuits. The array circuits have been fabricated using ITT-GTC's Multi-Function Self Aligned Gate process.**

I. INTRODUCTION

The design of microwave monolithic integrated circuits (MMICs) that efficiently generate high levels of power requires a high-performance fabrication process and accurate design techniques. Although microwave power design techniques are constantly being improved through non-linear modeling and EM simulation, design of an optimum circuit in one pass is rare. Statistical analysis is even more crude, with non-linear statistical analysis remaining beyond the reach of most microwave designers. Empirical design utilizing orthogonal array techniques can be used to supplement the circuit simulations with measurement-based circuit models. The purpose of this work is to show how proper application of both the latest microwave simulation and Taguchi orthogonal array experimentation techniques, implemented using a highly repeatable process [1], have been used to develop a robust power MMIC.

Recently reported power MMIC results have been largely based on PHEMT processes. Notable results achieved in C-band include those reported by White [2] and Brown [3]. The results obtained from this MESFET-based circuit compare favorably with published the PHEMT results; furthermore, the MSAG power FETs, operated at a drain voltage level of 10 volts, exhibit exceptional repeatability and reliability.

II. DESIGN

The nominal MMIC amplifier, shown in Figure 1, consists of 8 2.5mm MESFET cells reactively combined into a single stage. The chip dimensions are 6.5mm X 3.5mm. Each 2.5mm FET cell consists of sixteen 156μm long unit gate fingers arranged around 3 backside vias to lower the parasitic inductance. The port impedances are 25 ohms, thus reducing the MMIC matching circuit loss. The port impedances can be transformed using external circuitry such as a hybrid combiner. Drain bias is supplied through the RF output port. The gate bias may be applied either through the input RF port or through the pads connected to the first shunt stub on the input of each FET.

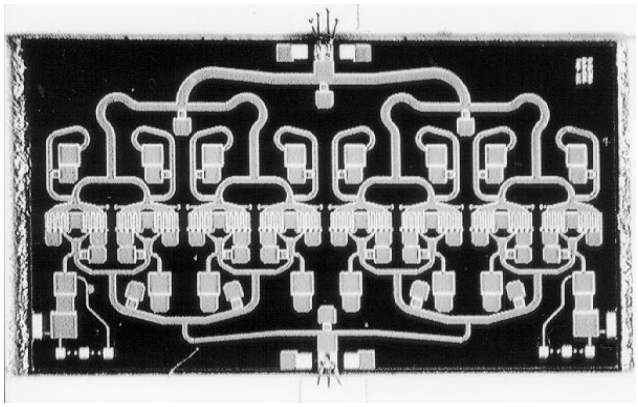

Figure 1: 13 W MMIC Amplifier Photograph

Although many approximations are needed to perform timely simulations of power MMICs, the models are constantly improving and accuracies of within 0.5 db in output power and 10% in efficiency are possible with nominally processed MMICs. Simulation of harmonic termination effects, a necessity in high efficiency power amplifier design, remains difficult. The design challenge arises when production specifications require better simulation accuracy and low manufacturing process sensitivity. Even the best simulation techniques are incapable of providing an adequate solution. In this instance, orthogonal array methodology provides the best solution to the problem of circuit design in the absence of simulation techniques. Circuit simulations are used to

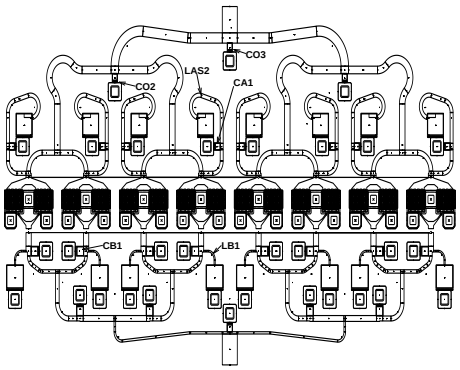

Figure 2: Nominal Circuit Layout

Table 1: Orthogonal Array Factors

FACTOR	LEVEL 1	LEVEL 2	LEVEL 3
A. FET	2.5mm	1.8mm	N/A
B. CB1	2.3 pF	2.0 pF	2.6 pF
C. LB1	NOM	$+35\mu m$	$-35\mu m$
D. CO2	1.1907 pF	1.47 pF	0.9408 pF
E. CO3	1.1907 pF	0.9919 pF	1.3669 pF
F. CA1	$1.2409pF$	$1.0092pF$	$1.5123pF$
G. LAS2	NOM	$+125\mu m$	$-125\mu m$
ERROR			

Table 2: Static Experiment Data

	VARIABLE							
	FET	CB1	LB1	CO2	CO3	CA1	LAS2	ERR
EXP	1	2	3	4	5	6	7	8
1	1	1	1	1	1	1	1	1
2	1	1	2	2	2	2	2	2
3	1	1	3	3	3	3	3	3
4	1	2	1	1	2	2	3	3
5	1	2	2	2	3	3	1	1
6	1	2	3	3	1	1	2	2
7	1	3	1	2	1	3	2	3
8	1	3	2	3	2	1	3	1
9	1	3	3	1	3	2	1	2
10	2	1	1	3	3	2	2	1
11	2	1	2	1	1	3	3	2
12	2	1	3	2	2	1	1	3
13	2	2	1	2	3	1	3	2
14	2	2	2	3	1	2	1	3
15	2	2	3	1	2	3	2	1
16	2	3	1	3	2	3	1	2
17	2	3	2	1	3	1	2	3
18	2	3	3	2	1	2	3	1

design a nominal circuit and to select the most sensitive circuit elements. These circuit elements are used as factors in an orthogonal array experiment with the factor levels carefully selected using circuit simulations. The entire array of circuits is fabricated using a "gate-array" mask to facilitate subsequent design changes. Each circuit is tested and standard orthogonal array analysis is used to select a circuit design which exhibits both high performance and process tolerance.

A Libra©layout of the nominal circuit is shown in Figure 2. The circuit has been optimized using a 2.5mm FET model scaled up from an existing 625μm FET non-linear model. The user-defined model is based on pulsed-IV characterization and S-parameters measured over a range of bias levels. The model has been verified using load-pull measurements and single-stage hybrid amplifier results. The 625μm model fit is good; however, this extensive scaling was expected to produce errors in prediction of parasitic elements. The non-linear model has also been used to select the most sensitive circuit elements and the range of variation for these elements to be included in the orthogonal array experiment. Selection of variables and ranges which form and adequate basis for the desired response space is crucial to the success of the experiment. Too little variation may not yield an optimum design whereas too much variation may result in marginal or non-functional amplifiers which invalidates interpolation between element values.

The circuit elements chosen for variation within the orthogonal array are marked with their respective names in Figure 2 keyed to the orthogonal array listed in Table 1. An 18 element orthogonal array is required for the seven variables at up to three levels. The element variations are shown by circuit in Table 2.

The basic assumption in the use of data from an orthogonal array for construction of an empirical model is that the effects of each of the individual elements of the array are mutually orthogonal. Circuit elements will interact in different ways across a given frequency band, especially at the band edges. Assuming that the non-linear model correctly predicts gradients, the goal is to center the design at a minimum point in the variable space so that movements can be approximated as linear combinations of the individual variables. This underscores the importance of the correct variable ranges. A column from the orthogonal array has been left blank in order to approximate the variable interactions [4]

III. RESULTS

The orthogonal array upon which this design is based consisted of 18 circuits arranged on a double reticle (9 circuits each, 12 circuits of each type on each wafer) for fabrication. One lot of wafers was fabricated from which an average wafer was selected for fixtured power testing. All three PCM-good wafers from the first lot have been pulse tested. The on-wafer data for all parts of the selected type (circuit 1) from the first lot appears in Figure 3. The spread of less than 0.5 dB in output power demonstrates the repeatability of the MSAG process. Some discrepancy between measured wafer and fixtured test data has been traced to circuit loading problems on-wafer resulting from the 25Ω port impedances.

The orthogonal array analysis is based on an at least five parts of each circuit type, taken from a single wafer,

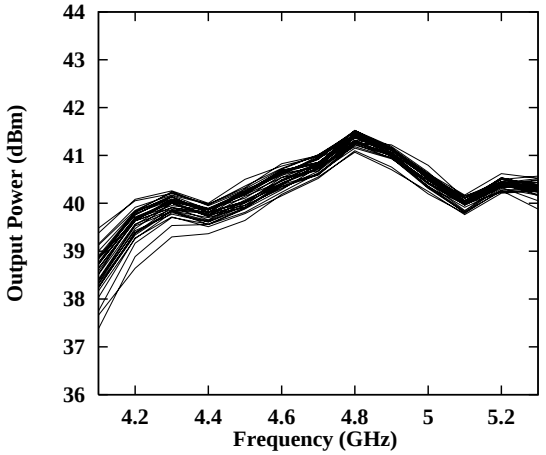

Figure 3: Pulsed On-wafer MMIC Performance

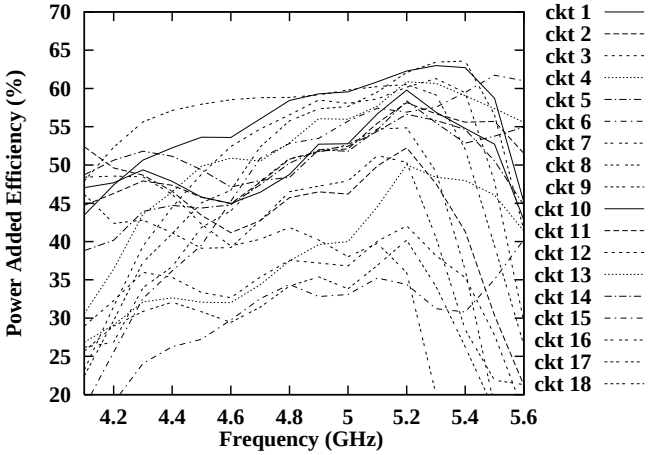

Figure 4: Experimental Circuit Measurements

fixtured with impedance transformers to facilitate 50Ω testing. The average PAE at a fixed input power level has been measured for each circuit and plotted in Figure 4 in order to show the range of the orthogonal array variables. The non-linear model predicted less variation than is shown in Figure 4, with some of the PAE results (less than 40considered to be on the borderline of functionality. This wide range of responses will be shown to have an adverse effect on the prediction of optimum circuit performance.

The figure-of-merit chosen for the orthogonal array analysis is a modified form of the amplifier efficiency calculation. The power-added efficiency calculation is shown in equation (1) below.

$$PAE = \frac{P_{rf-out} - P_{rf-in}}{V_{dc} * I_{dc}} \tag{1}$$

Cubic splines are generated from the data for each circuit so that the amplifier PAE at a fixed output power level can be determined. If a given circuit fails to produce the required output power level, a continuous penalty function is applied which tries to assign an efficiency level to the circuit if it could be driven hard enough to produce the proper output power level. The assumption is that drain current remains fixed and that the output power increases 0.22 dB for each 1 dB increase in the input signal level. Based on equation 1, this increased input signal level severely reduces the amplifier PAE. The rationale behind this approach is that an ideal amplifier would produce the required output power at the highest possible efficiency. The output level used in the analysis, 40.7 dBm, is chosen to size the amplifier for its application.

This "corrected PAE" data is calculated for each circuit under all test conditions. The data is then used to form a single larger-the-better S/N ratio [4] value for

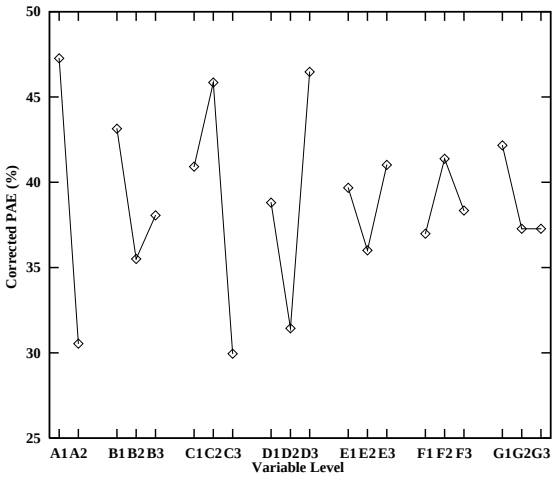

Figure 5: Orthogonal Array Response Plots

each circuit type that includes all of the tested circuits of that type (5 to 6 based on functional test yield) and all frequency values. The S/N ratio (η) calculation is given in equation (2).

$$\begin{aligned} \eta &= -10log_{10}[\frac{1}{n}\sum_{i=1}^{n}\frac{1}{y_i^2}] \\ n &= num\ parts\ tested * num\ freq\ pnts \\ y &= amplifier\ corrected\ PAE \end{aligned} \tag{2}$$

The noise factors, process variation and input signal frequency, are implicitly included in this calculation. Optimizing this S/N ratio provides the best performance and robustness against process variation. A "response plot" for each variable appears in Figure 5. The response is the average effect of each variable on the S/N ratio from the orthogonal array results. This plot shows the optimum level for each variable and its relative effect on the circuit response.

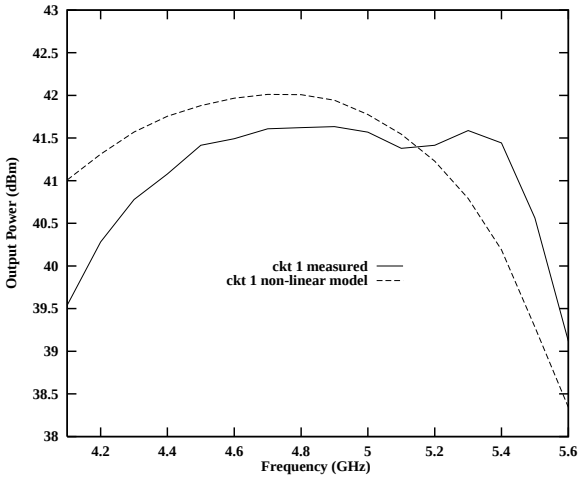

Figure 6: Non-linear Output Power Prediction Comparison

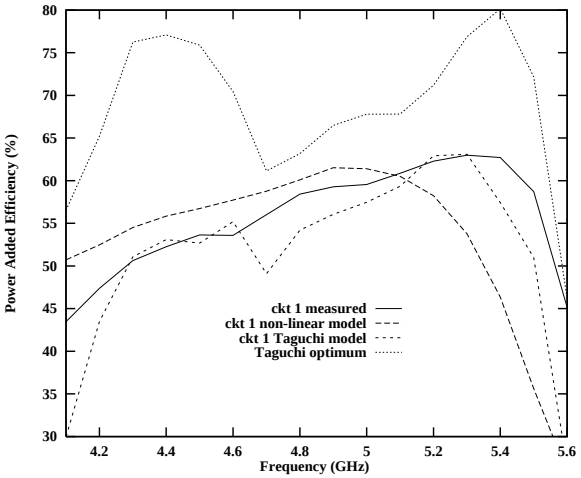

Figure 7: Comparison of simulated, measured and Taguchi optimum PAE

The plots of Figure 5 show that FET size, input stub length LB1, and output capacitor CO2 are the dominate variables in this frequency-independent analysis. The FET size and load-line slope (predominately determined by CO2) obviously must be chosen correctly to produce the relatively high output power (40.7 dBm) required from the chip. Variable LB1 varies both the input match and the input second harmonic termination. Harmonic terminations consistently figure heavily in results of orthogonal array experiments conducted in this frequency range. Although the non-linear model predicts some harmonic termination dependence, it is based on non-linear capacitance formulations which are crude approximations at best. These variables can only be fine tuned in an experimental manner.

The orthogonal array analysis shows two circuits from the 18 experiments which provide good power and efficiency over the measured bandwidth. Neither of these circuits, numbers 1 and 8, contain the optimum levels of all variables as selected from the response plots of Figure 5. A plot of the average output power from five fixtured circuit 1 amplifiers is shown in Figure 6. The non-linear model prediction is also included. The discrepancy arises from incorrect parasitic scaling and incorrect prediction of harmonic termination effects. The circuit design was optimized for both power and efficiency with circuit 1 being the optimum modeled circuit. Two orthogonal array Taguchi model responses also appear in Figure 7. The Taguchi model curve is generated by using the variable levels from circuit 1 in the Taguchi model. The Taguchi optimum curve is generated using the optimum variable levels as selected from Figure 5. Although the Taguchi optimum circuit, which has not yet been fabricated, will obviously not produce the PAE level shown, it suggests that significant improvement is possible. The over-estimate of the PAE is likely a result of the excessive range of the experiment variables. The Taguchi optimum circuit is currently in fabrication.

IV. CONCLUSIONS

A state-of-the-art high-efficiency power amplifier design utilizing the MSAG ion-implanted process has been fabricated and the results have been presented. Data from MMICs measured across one lot of wafers demonstrate that the design can be manufactured with tight specification tolerances. Orthogonal array techniques have been applied to show the process tolerance of the design as well as showing that the non-linear model was insufficient to optimize the design for power and efficiency.

References

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